SPICE Modeling of SiC MOSFET Considering Interface-Trap Influence

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Abstract—SPICE modeling of silicon carbide (SiC) MOSFET considering the influence of interface traps has been carried out, which is able to describe the characteristics of the MOS transistors in all operation modes at different interface trap densities and measurement temperatures. This modeling employs the SPICE level-1 model of MOSFET, but the constant mobility in the piecewise current equations has been replaced by the advanced mobility expression, which can exactly reflect the effect of SiC/SiO₂ interface traps on the electrical characteristics of SiC MOSFET. Key parameters in the advanced mobility model are obtained according to charge-sheet model (CSM) of MOS system. The static characteristics of the developed SiC MOSFET model have been validated with the production Datasheet, and the dynamic characteristics have been experimentally verified in Boost converter. Based on the developed model, the effect of SiC/SiO₂ interface-trap densities on the switching performances of SiC MOSFET has been quantitatively discussed, and reasonable gate driving voltage of SiC MOSFET with different interface-trap densities has been revealed.

Index Terms—Interface traps, mobility, SiC MOSFET, SPICE modeling, switching loss.

I. INTRODUCTION

RECENTLY, significant efforts have been made to improve the performance efficiency of semiconductor devices applied in power conversion systems. The wide band-gap (WBG) material silicon carbide (SiC) has demonstrated great promise to improve the limitations associated with the current rate of the technology for silicon (Si) power devices [1], [2]. SiC can provide satisfactory performance under high switching frequency applications [3]-[6], thus enabling the use of smaller filter components within the converter circuits. This points to the ability of power devices based on SiC to potentially optimize the power density of next generation power converters [7]. Furthermore, SiC power devices can also sustain high operating temperatures, thus making them attractive candidates for applications in aircraft, automotive, and energy exploration industries, etc [8], [9].

Thanks to recent progress in SiC process technology, SiC MOSFET has been commercialized. It can be predicted that SiC MOSFET will be applied in power converters more and more widely as its price continually decreases. Therefore, an accurate model of SiC MOSFET is necessary for device evaluation, system design, and power converter behavior prediction. Mantooth et al., reviewed different compact models of SiC MOSFET developed by many research groups [10]. The categorization and characteristics of different modeling methods on power semiconductor devices were also reported in this literature. Some effects were considered in these models, such as temperature-dependent gate threshold voltage, temperature-dependent carrier mobility, nonuniform current distribution, and so on [11]-[13]. Another important characteristic of trap density at the SiC/SiO₂ interface was also included in some SiC MOSFET models. Potbhare et al., developed a comprehensive physical model of 4H-SiC MOSFET, which incorporated interface trap densities and Coulombic interface trap scattering, surface roughness scattering, phonon scattering, velocity saturation, and their dependences on bias and temperature [14]. The physics-based models were implemented into a device simulator that is tailored for 4H-SiC MOSFET analysis, and not suitable for circuit simulations and practical applications due to its high complexity. Tanimoto et al., developed a compact SiC MOSFET model for circuit simulation by considering the trap density, which is included in the Poisson's equation. The model is constructed in HiSIM_HV, a power MOSFET model developed by Hiroshima University based on surface-potential based MOSFET model [15]. Kraus et al., developed a physics-based compact model of SiC MOSFET including the dependence of channel charge and electron mobility on the charge of interface traps in circuit simulator PSpice [16]. However, many fitting parameters were used in this model, and the effect of interface traps can not be obviously found in the expressions which describe the behavior of SiC MOSFET. In this paper, SPICE modeling of SiC MOSFET is carried out in LTspice IV, a high performance SPICE simulator and free of charge. The model is developed for an example device C2M0080120D (1200 V/36 A SiC MOSFET from Cree, Inc). Advanced mobility model is introduced to describe the interface characteristics and temperature on the effect of the electrical performance of SiC MOSFET. The static characteristics are validated with C2M0080120D Datasheet, and dynamic characteristics are verified by the experimental tests on a Boost converter platform.

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II. SPICE MODELING OF SIC MOSFET WITH INTERFACE TRAPPED CHARGE

A. Review on Previous SPICE Modeling for SiC Power MOS-FET Based on Their Deficiencies

Fig. 1 shows the equivalent sub-circuit model of SiC MOS-FET, which is employed in some literatures [11], [12], [17]. The model consists of nine components. M_1 : the built-in SPICE level-1 MOSFET, D_1 : the body diode, and its junction capacitor is used as drain-source capacitor C_{DS} of SiC MOSFET, R_G : gate resistor, R_S : source resistor, R_D : drain resistor, C_{GS} : gatesource capacitor, C_{GD} : gate-drain capacitor, E_{TEMP} : temperature-dependent voltage source, G_{TEMP} : temperature-dependent current source. The above components play different roles in the operation of SiC MOSFET. M_1 is used to describe the MOS channel. R_D , R_S , and the resistance of M_1 are used to describe the on-state resistance of SiC MOSFET. E_{TEMP} and G_{TEMP} are employed to describe the static characteristics of SiC MOSFET. C_{GD} and C_{GS} are used to describe the dynamic characteristics. Based on the model shown in Fig. 1, Sun et al., simulated some temperature-dependent effects of SiC MOSFET, such as positive or negative temperature coefficient, threshold voltage and transconductance variations with temperature [12]. Wang et al., claimed the application of this model to describe the temperature-dependent characteristics of the SiC MOSFET, particularly the effects induced by the high density of interface traps present at SiC/SiO₂ interface [11], [17], however, the detailed methodology on how to incorporate the effect of interface traps can not be found in the literatures.

The built-in SPICE level-1 component, M_1 , is based on Shichman-Hodges' physical model, which represents the behavior of the device in different modes of operation with simple analytical equations. Equation (1) defines the cutoff region, (2) is the linear region, and (3) is the saturation region, and five parameters are used, they are carrier mobility (μ), channel width (W), channel length (L), threshold voltage (V_{TH}), and channel length modulation parameter (λ), respectively.

$$I_{DS} = 0, if V_{GS} < V_{TH} .$$
 (1)

$$I_{DS} = \mu C_{ox} \frac{W}{L} [(V_{GS} - V_{TH}) \cdot V_{DS} - \frac{1}{2} V_{DS}^2] \cdot (1 + \lambda V_{DS}),$$

if $V_{GS} > V_{TH} \& V_{DS} < V_{GS} - V_{TH}$. (2)

$$I_{DS} = \frac{\mu C_{ox}}{2} \frac{W}{L} (V_{GS} - V_{TH})^2 \cdot (1 + \lambda V_{DS}),$$

if $V_{GS} > V_{TH} \& V_{DS} > V_{GS} - V_{TH}$. (3)

B. The Novel Model Considering Interface-Trap Influence Based on the Advanced Mobility Expression

The SPICE level-1 model of MOSFET is available in many circuit simulation tools, such as PSpice and Saber, and the



Fig. 1. SPICE sub-circuit model of SiC MOSFET in [11] and [12].

model can satisfactorily meet the requirement in accuracy and time consumption. Nevertheless, SPICE level-1 model was originally developed for Si-based devices, and the carrier mobility was constant, this is for the reason that Si MOSFET has a high-quality interface of Si/SiO₂, and the interface issue on the effect of electrical characteristics of Si MOSFET did not need to be considered. For SiC-based MOS devices, however, the very high density of traps at the SiC/SiO₂ interface bring strongly effect on the electrical characteristics of SiC MOSFET [18]. Interface traps can capture carriers in the inversion channel of SiC MOSFET, which leads to the decreasing of on-state current and the increasing of the on-state resistance. Then, the occupied traps become charge centers, which forms Coulombic scattering and lowers the mobility of carriers in channel.

Besides, the mobility degradation of carriers in inversion layer also comes from other scatterings, which are bulk lattice scattering, acoustic phonon scattering, and roughness scattering, respectively. Together with Coulombic scattering, the four different scatterings correspond to four different mobility components. According to Mathiessen's rule, the inversion mobility of carrier μ_{inv} is defined by [14], [19]-[22]

$$\frac{1}{\mu_{inv}} = \left(\frac{1}{\mu_B} + \frac{1}{\mu_{AC}} + \frac{1}{\mu_{SR}} + \frac{1}{\mu_C}\right).$$
 (4)

In (4), μ_B is bulk lattice scattering, μ_{AC} is acoustic phonon scattering, μ_{SR} is surface roughness scattering, and μ_C is Coulombic scattering. The corresponding expressions for four different scatterings are summarized in TABLE I [21].

In TABLE I, empirical values of parameters in the four mobility expressions are also listed. E_{\perp} in μ_{AC} and μ_{SR} is the effective perpendicular electric field at the interface. T, Q_{inv} and Q_{irap} in μ_C are the temperature, inversion charge and trapped charge, respectively.

The effect of interface traps on electrical characteristics of SiC MOSFET is reflected by Coulombic scattering μ_C . If more carriers are trapped, which means that Q_{trap} is higher and Q_{inv} is lower, μ_C would become lower. Under low-field operation of SiC MOSFET, the inversion mobility μ_{inv} is determined by μ_C . Therefore, if we use μ_{inv} in (4) to replace constant mobility in SPICE level-1 MOSFET model, the effect of interface traps on

 TABLE I

 Four Mobility Components and Their Parameter Values

Mobility	Expression	Value	
μ_B	$\mu_{\min} + \frac{\mu_{\max} - \mu_{\min}}{1 + \frac{N_A}{N_{\text{REF}}}}$	$\mu_{\rm max} = 950 \text{ cm}^2/\text{Vs}$ $\mu_{\rm min} = 40 \text{ cm}^2/\text{Vs}$ $N_{\rm A} = 1 \times 10^{16} \text{ cm}^{-3}$ $N_{\rm REF} = 2 \times 10^{17} \text{ cm}^{-3}$	
μ_{AC}	$\frac{B}{E_{\perp}} + \frac{CN_{A}^{a1}}{TE_{\perp}^{1/3}}$	$B = 1.0 \times 10^{6} \text{ cm/s}$ $\alpha 1 = 0.0284$ $C = 3.23 \times 10^{6} \text{K cm/s (V/cm)}^{-23}$	
μ_{SR}	$rac{D_1}{E_\perp^2}$	$D_1 = 5.82 \times 10^{14} \text{ cm}^2/\text{V s} (\text{V/cm})^2$	
μ_{C}	$NT^{lpha}rac{{\cal Q}_{inv}^{\ eta}}{{\cal Q}_{trap}}$	$\alpha = 1$ $\beta = 1$ $N = 0.007525 \text{ cm}^2/\text{V s}$	

electrical characteristics of SiC MOSFET can be assessed, and we can quantitatively investigate the effect of different interface-trap density on the switching behaviors of SiC MOSFET.

C. The Modeling for Field and Temperature Dependence Based on Charge-Sheet Model of MOS System

The effective electric field E_{\perp} and inversion charge Q_{inv} can be obtained according to charge-sheet model (CSM) of MOS system. The charge-sheet model is widely used for calculating the dependence of inversion-layer charge density on surface potential, thus serves as a starting point for describing the current transport in a MOS transistor. The model simplifies the calculation of the inversion charges by assuming that the inversion layer is a charge sheet of infinitesimal thickness, so that the inversion charge Q_{inv} is simply the difference between the total space charge Q_{sc} in the surface space-charge region and the charge within the depletion layer Q_{dep} (in units of cm⁻²)

$$Q_{inv} = Q_{sc} - Q_{dep} . ag{5}$$

The charge-sheet model equations are also used to calculate the effective electric field in the inversion layer. The effective field in the inversion layer has been reported in [19] to be (ε_s is the permittivity of SiC)

$$E_{\perp} = 1/\varepsilon_s \left(1/2Q_{inv} + Q_{dep}\right). \tag{6}$$

Detailed procedure of calculating inversion-layer charge densities of Q_{sc} and Q_{dep} can be found in [21], [23], [24]. Q_{sc} and Q_{dep} are both dependent on surface potential Φ_s , and Φ_s is related with gate voltage and given by an implicit function [25]

$$V_{GB} - V_{FB} - \Phi_{S} = \gamma \sqrt{\Phi_{S} - \varphi_{t} + \varphi_{t} \cdot \exp[(\Phi_{S} - 2\Phi_{F} - V_{CB})/\varphi_{t}] + \varphi_{t} \cdot \exp(-\Phi_{S}/\varphi_{t})}.$$
 (7)

In this expression, V_{GB} is the applied voltage between gate and bulk, V_{FB} is flat band voltage, γ is bulk effect coefficient, φ_t is thermal voltage and expressed by kT/q, V_{CB} is the voltage be-



Fig. 2. Proposed SPICE sub-circuit model of SiC MOSFET in this work.

tween channel and bulk. If some parameters are given, such as the material parameters, physical dimensions and doping concentrations of MOS device, according to CSM model, E_{\perp} and Q_{inv} are only the function of gate voltage and temperature. And so, the inversion mobility μ_{inv} can be determined by interface trapped charge Q_{trap} for given gate voltage and temperature. In [11] and [12], the temperature-dependent effects are described by E_{TEMP} and G_{TEMP} . In [16], authors also asserted that the influence of a variable temperature on the model parameters is taken into account, but none of parameters in the model can be found to be temperature-dependent, only a thermal equivalent circuit is used to simulate the self-heating. In our model, these effects are described by the temperature-dependent mobility components μ_{AC} and μ_{C} , temperature-dependent threshold voltage (expressed by 2.437-0.0057*T, obtained by fitting with C2M0080120D datasheet), so we removed E_{TEMP} and G_{TEMP} in Fig. 1, and the equivalent sub-circuit model in this work is shown in Fig. 2.

Aside from the Coulombic scattering, roughness scattering also brings strongly influences on the carrier mobility. In [16], the influence is claimed to be included in the current equation, but is not explicitly accounted for. In our model, the roughness scattering is directly related with the effective perpendicular electric field. Increasing gate voltage means the increasing of effective perpendicular electric field E_{\perp} , so the roughness scattering becomes much stronger, which will promote the degradation of carrier mobility.

In [15], the transient SiC MOSFET behavior is reflected by the dynamic trap charges, and the time constants for trapping and detrapping process are the function of time and gate voltage. Comparatively, in our model, the transient behavior of SiC MOSFET is reflected by the action of interface traps on the inversion carriers, which should be more reasonable for the role of interface traps in the operation of SiC MOSFET.

D. The Simplified Model for Gate-Drain Capacitance(C_{GD})

Capacitance between electrodes can storage charge, which can impose effects on the dynamic performance of SiC MOS-FET. Three capacitors, C_{GD} , C_{GS} and C_{DS} are used to model the effect. In this model, C_{GD} is modeled based on "switching model" SIEMES [17], but we simplify it by a voltage-dependent current source, and the structure is shown in Fig. 3. In this fig-



Fig. 3. Simplified C_{GD} model in this work.



Fig. 4. Comparison of C_{GD} between a simplified model and C2M0080120D Datasheet.

ure, G_{GD} is voltage-controlled current, and is used to represent the C_{GD} when gate-drain voltage (V_{GD}) is less than or equal to 0. C_{GDM} is constant, and represents C_{GD} when V_{GD} is greater than 0. We fit this C_{GD} model with C2M0080120D datasheet [26], and get a new expression for C_{GD} .

$$\begin{cases} G_{GD} = \left(\frac{a}{\left(1 - \frac{V_{GD}}{b}\right)^c} - a\right) \frac{dV_{GD}}{dt}, \quad V_{GD} \le 0 \\ G_{GD} = 0, \quad V_{GD} > 0. \end{cases}$$

$$\tag{8}$$

Here, *a*, *b*, *c* are all constants, and with the values of 0.40110 e-9, 8.34, and 2.29, respectively. The comparison between C2M00 80120D datasheet and C_{GD} model is shown in Fig. 4.

Compared to the high nonlinearity of C_{GD} , another two capacitors, C_{GS} and C_{DS} , are little affected by the operation of SiC MOSFET, and are modeled by a constant capacitor respectively.

We successfully realized the calculation of E_{\perp} , Q_{inv} , Q_{sc} and Q_{dep} in circuit simulator LTspice IV by means of the so-called Arbitrary Behavioral Sources (ABS). After obtaining the inversion mobility μ_{inv} according to (4), we used μ_{inv} to replace the



Fig. 5. Comparison of transfer characteristics between this developed SPICE model with C2M0080120D Datasheet.

constant mobility μ in (2) and (3). So, the M_1 in Fig. 2 is characterized with the integration of interface trapped charge Q_{trap} and temperature *T*, and the effects of Q_{trap} and *T* on the electrical characteristics of SiC MOSFET can be discussed.

III. VERIFICATION OF DEVELOPED SIC MOSFET MODEL

A. Static Characteristics Verification

The static characteristics of this developed Spice model are validated against the existing SiC MOSFET C2M0080120D Datasheet [26]. The comparisons of transfer characteristics and output characteristics between the measured results from the Datasheet and the simulation results by the proposed model at 25 °C and 150 °C are shown in Fig. 5 and Fig. 6. One can see that a reasonable agreement was achieved between the proposed model and the Datasheet, especially the transfer characteristics. Although a deviation appeared for higher gate bias in Fig. 6, however, it is normal and also occurs in other's work [27], [28]. Compared to the physical model of power device, Spice model employs segmented expressions to describe the channel current, more complex physical effect, especially under high field and high temperature, is hardly included into Spice model.

B. Dynamic Characteristics Verification

The dynamic characteristics are verified by experimental results in Boost converter. The schematics of the converter in LTspice IV simulator and the test platform are shown in Fig. 7, respectively. The freewheeling diode (FWD) in the Boost converter is SiC schottky barrier diode (SBD) C4D10120A from Cree. The model of C4D10120A in the simulation is developed by Cree for LTspice IV. Circuit parameters are listed in TABLE II. V_{GS} is the gate-source voltage, V_{DC} is the input voltage of Boost converter, f is the switching frequency, and D represents the duty cycle. All the parameters are same except that the inductance in LTspice IV is 0.01 mH higher than the one in experimental prototype, this is a consideration of the parasitic inductance in experiment circuit.

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Fig. 6. Comparison of output characteristics between this developed SPICE model with C2M0080120D Datasheet at 25 $^\circ$ C (a) and 150 $^\circ$ C (b).





Fig. 7. Schematic of Boost converter in LTspice IV (a) and the experimental platform (b).

TABLE II Parameters in Boost Converter for LTspice IV and Experiment

Symbol	Name -	Description		
		Experiment	LTspice IV	
V_{I}	V_{GS}	V _{GS} =20 V, <i>f</i> =130 kHz, <i>D</i> =62%	<i>V_{GS}</i> =20 V, <i>f</i> =130 kHz, <i>D</i> =62%	
V_2	V_{DC}	180 V	180 V	
L	Inductance	0.5 mH	0.51 mH	
М	SIC MOSFET	C2M0080120D from Cree	Developed model in this paper	
D	SiC SBD	C4D10120A from Cree	SPICE model from Cree	
С	Capacitance	2 μF	2 µF	
R	Resistance	290 Ω	290 Ω	



Fig. 8. Comparison of turn-on (a) and turn-off (b) waveforms at 470 V between LTspice IV simulation and experiment in Boost converter.

Carefully correlating the number of interface trapped charge, when Q_{trap} is set to 1.39×10^{12} cm⁻², reasonable agreement in switching waveforms is obtained between the measured data and the proposed model, which is shown in Fig. 8. At the same time, the results of so-called previous model with a constant mobility are also plotted in Fig. 8 as a reference. One can see that a larger mismatch appears between the measured data and the previous model. In the modeling, to model the stray inductance introduced by cables and connections, a small inductance,



Fig. 9. Comparison of turn-on (a) and turn-off (b) waveforms at 800 V between LTspice IV simulation and experiment in Boost converter.

with a value of 7 nH, was placed at the anode of freewheeling diode (not shown in Fig. 7(a)). The value was chosen according to the voltage overshoot measured across the MOSFET during its turning off.

The switching voltage of SiC MOSFET in Fig. 8 is 470 V, to furthermore verify the accuracy of the proposed model, a comparison of higher switching voltage with 800 V was made, and results are described in Fig. 9. Although relatively large deviation occurs, the model can still reproduce the experimental results.

In the simulation of Boost converter, rated with 180 V input voltage, 130 kHz switching frequency and 62% duty cycle, the consumption time of running 100 periods is about 225 s. If we only save hundredth waveform, the consumption time is about 75 s, which is acceptable for power circuit simulation.

IV. Application of the Developed Model in Power Circuit

An important application of the model is to predict the effect of interface traps on the electrical characteristics of SiC MOS-FET in power circuits. The issue of power device in circuit is the switching loss, which can determine the working efficiency of power equipments. In this paper, a clamped inductive switching circuit is employed to evaluate the electrical behavior of the



Fig. 10. Clamped inductive switching circuit for simulation of SiC MOS-FET's switching loss.

developed SiC MOSFET model with different interface trap densities, and the schematic is shown in Fig. 10. The component parameters are also marked in the schematic. For the gate driving of SiC MOSFET, a step pulse with 1 μ s width and 3 μ s period is biased to gate electrode through a 10 Ω resistance.

Generally, interface trap can be classified into two types: the acceptor-like trap, located in the upper half of the energy gap, and the donor-like trap, located in the lower half of the energy gap. For *n*-channel MOSFET, playing dominative role is the acceptor-like trap, empty acceptor-like trap is neutrality, and can be negatively charged after capturing an electron. At present, the commercial SiC MOSFET has been believed to be annealed in NO at 1175 °C to decrease the density of interface trap. Here, three different distributions of interface acceptor-like trap have been taken to assess the effect of interface traps on the electrical characteristics of SiC MOSFET. Three distributions shown in Fig. 11 are picked from [29], and obtained in NO annealing at 1175 °C with different time.

For a continuous energy distribution of interface traps, the trapped charges may be approximated by following expression [21].

$$Q_{trap} = \int_{E_i}^{E_c} D_{it}(E,T) dE .$$
(9)

Where, E_i is the intrinsic energy. Q_{trap} corresponding to three distributions of interface trap is 2.87×10^{11} cm⁻², 1.83×10^{12} cm⁻², 1.63×10^{13} cm⁻², respectively, and successively named Q_{trap0} , Q_{trap1} , Q_{trap2} .

The switching waveforms of SiC MOSFET in Fig. 10 corresponding to Q_{trap0} , Q_{trap1} and Q_{trap2} are shown in Fig. 12. It can be seen that interface traps delay the turn-on of SiC MOSFET, and lead the device forward to turn-off in advance. For *n*-channel MOSFET, acceptor-like traps capture the free electrons in the channel, resulting in the decreasing of drain-source current, and more traps mean less electrons. Also, the charged traps become the scattering centers, hindering the movement of electrons, so the rising of the drain-source current I_{DS} and the falling of drainsource voltage V_{DS} both becomes slow during the turn-on of SiC MOSFET. After the gate voltage is removed, the device with higher density of interface traps can turn off more early as a

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Fig. 11. Three distributions of interface traps for LTspice simulation [29].

Fig. 12. Switching waveforms of SiC MOSFET for different Q_{trap} .

result of more electrons captured. The simulated results of interface trap's influence on the switching behavior of SiC MOSFET can bring prompt for device application in series or in parallel to improve its power capacity. Synchronization of device operation is required for this application, so these devices should be with the same density of interface traps to avoid the out-of-step in turning-on and turning-off.

The turn-on loss, turn-off loss and total loss of SiC MOS-FET for three distributions of interface traps are also calculated by the product of V_{DS} and I_{DS} , the results are listed in TABLE III. We can see that the turn-on and turn-off losses both increase with the increasing density of interface trap. The interface traps delay the turn-on of 4H-SiC MOSFET and the overlapping region of V_{DS} versus I_{DS} increases, which leads to a higher power loss. Though the interface traps drive the device turn-off in advance, the overlapping region also increases with the density of interface traps, so the turn-off loss increases. Higher density of interface traps capture more carriers in the channel, and so the on-state resistance increases.

Extensive application of this developed model is to assess the effect of gate driving voltage on the loss of SiC MOSFET with different distributions of interface traps. We know, higher gate voltage can yield more free carriers in the inversion layer of channel, which can decrease the switching loss and on-state

TABLE III The Loss of SiC Mosfet for Different Q_{trap}

Q_{trap} (cm ⁻²)	Turn-on Loss (W)	Turn-off Loss (W)	Total Loss (W)
$Q_{trap0} = (2.87 \times 10^{11})$	17.58	19.74	52.16
Q_{trapl} (1.83×10 ¹²)	20.51	20.43	56.35
Q_{trap2} (1.63×10 ¹³)	37.28	22.30	84.72

Fig. 13. Relationship between gate voltage and the total loss of SiC MOS-FET with different interface traps.

loss, but rise the complexity and the loss of gate driver. However, when the density of interface traps is high, increasing gate voltage seems to be an effective method to decrease the switching loss and on-state loss. Fig. 13 shows the relationship between gate voltage and the total loss of SiC MOSFET for three distributions of interface traps. The first noticed point is that the switching loss is very high when the gate voltage is less than 20 V, but shows less change for gate voltages higher than 20 V. This model is developed taking the C2M0080120D device as example, and the suggested gate voltage in C2M0080120D Datasheet is 20 V, which is consistent with our simulation result, the loss and gate driving complexity can obtain a good tradeoff under this voltage.

V. CONCLUSIONS

A novel circuit simulation model of SiC MOSFET is proposed and validated. The model is developed based on the present SPICE level-1 MOSFET model, but the constant mobility has been replaced by advanced mobility which can reflect the effect of interface traps and temperature on the electrical behavior of SiC MOSFET. The including of interface traps in this model makes it suitable for simulating the synchronization of device operation in series or parallel connection, also, the loss of SiC MOSFET can be accurately assessed by applying this model in the design of power converters.

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